In the Claims

Claims 32-56 are pending in the application with claims 32, 36, 40, and 45 amended herein and new claims 53-56 added herein.

Claims 1-31 (cancelled)

32. (currently amended) A capacitor construction comprising a first capacitor electrode over a substrate, a capacitor dielectric layer over the first electrode, a second capacitor electrode over the dielectric layer, and an atomic layer deposited insulative barrier layer to oxygen diffusion between the first electrode and the dielectric layer and/or between the dielectric layer and the second ~~electrodes~~ electrode.

33. (previously presented) The construction of claim 32 wherein the barrier layer has a thickness of less than about 12 Angstroms.

34. (previously presented) The construction of claim 32 wherein the barrier layer comprises Al_2O_3.

35. (previously presented) The construction of claim 32 wherein the barrier layer exhibits a K factor of greater than about 7 at 20° C.

36. (currently amended) A capacitor construction comprising:

a first capacitor electrode over a substrate;

an insulative barrier layer to oxygen diffusion over the first electrode, the barrier layer comprising a chemisorption product of first and second substantially saturated precursor monolayers;

a capacitor dielectric layer over the barrier layer or between the first electrode and the barrier layer; and

a second capacitor electrode over the dielectric layer and the barrier layer.

37. (previously presented) The construction of claim 36 wherein the barrier layer has a thickness of less than about 12 Angstroms.

38. (previously presented) The construction of claim 36 wherein the barrier layer comprises Al_2O_3.

39. (previously presented) The construction of claim 36 wherein the barrier layer exhibits a K factor of greater than about 7 at 20° C.

40. (currently amended) A memory array comprising:

a plurality of capacitor constructions each having a first capacitor electrode over a substrate, a capacitor dielectric layer over the first electrode, a second capacitor electrode over the dielectric layer, and an atomic layer deposited insulative barrier layer to oxygen diffusion between the first electrode and the dielectric layer and/or between the dielectric layer and the second ~~electrodes~~ electrode.

41. (previously presented) The array of claim 40 wherein the barrier layer has a thickness of less than about 12 Angstroms.

42. (previously presented) The array of claim 40 wherein the barrier layer comprises Al_2O_3.

43. (previously presented) The array of claim 40 wherein the barrier layer exhibits a K factor of greater than about 7 at 20° C.

44. (previously presented) The array of claim 40 wherein the barrier layer comprises a chemisorption product of first and second substantially saturated precursor monolayers.

45. (currently amended) A plurality of memory dice, each die comprising:

a section of a monocrystalline semiconductor wafer; and

a capacitor construction comprising a first capacitor electrode over the wafer, a capacitor dielectric layer over the first electrode, a second capacitor electrode over the dielectric layer, and an atomic layer deposited insulative barrier layer to oxygen diffusion between the first electrode and the dielectric layer and/or between the dielectric layer and the second ~~electrodes~~ electrode.

46. (previously presented) The dice of claim 45 wherein the barrier layer has a thickness of less than about 12 Angstroms.

47. (previously presented) The dice of claim 45 wherein the barrier layer comprises Al_2O_3.

48. (previously presented) The dice of claim 45 wherein the barrier layer exhibits a K factor of greater than about 7 at 20° C.

49. (previously presented) The dice of claim 45 wherein the barrier layer comprises a chemisorption product of first and second substantially saturated precursor monolayers.

50. (previously presented) The array of claim 44 wherein the first and second precursors are different.

51. (previously presented) The dice of claim 49 wherein the first and second precursors are different.

52. (previously presented) The construction of claim 36 wherein the first and second precursors are different.

53. (new) The construction of claim 32 wherein the barrier layer is between the dielectric layer and the first electrode.

54. (new) The construction of claim 36 wherein the dielectric layer is over the barrier layer.

55. (new) The array of claim 40 wherein the barrier layer is between the dielectric layer and the first electrode.

56. (new) The dice of claim 45 wherein the barrier layer is between the dielectric layer and the first electrode.